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PRE-APPEAL BRIEF REQUEST FOR REVIEW

Docket Number (Optional)	
SCS-550-525	

Application Number	Filed
10/779,808	February 18, 2004
First Named Inventor: GILKERSON	
Art Unit: 2183	Examiner: R. Fennema

Applicant requests review of the final rejection in the above-identified application. No amendments are being filed with this request.

This request is being filed with a notice of appeal.

The review is requested for the reason(s) stated on the attached sheet(s).
Note: No more than five (5) pages may be provided.

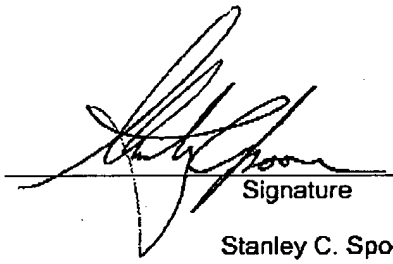
I am the

☐ Applicant/Inventor

☐ Assignee of record of the entire interest. See 37 C.F.R. § 3.71. Statement under 37 C.F.R. § 3.73(b) is enclosed. (Form PTO/SB/96)

☒ Attorney or agent of record 27,393 (Reg. No.)

☐ Attorney or agent acting under 37CFR 1.34.
Registration number if acting under 37 C.F.R. § 1.34 _____



Signature

Stanley C. Spooner

Typed or printed name

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Requester's telephone number

January 26, 2007

Date

NOTE: Signatures of all the inventors or assignees of record of the entire interest or their representative(s) are required. Submit multiple forms if more than one signature is required, see below.*

☒ *Total of 1 form/s are submitted.

STATEMENT OF ARGUMENTS IN SUPPORT OF PRE-APPEAL BRIEF REQUEST FOR REVIEW

Error #1. The Furber prior art, where there is an instruction flow changing instruction [IFCI], does not teach a determination between two address generation paths based upon the IFCI being a first prefetched instruction

Applicant's independent claims 1, 11 and 21 recite address generation logic within the prefetch unit "having a first address generation path for determining the target address **if** the selected prefetched instruction is a first prefetched instruction in said plurality, and at least one further address generation path for determining the target address **if** the selected prefetched instruction is one of the other prefetched instructions in said plurality." (emphasis added). The Examiner alleges that the claimed apparatus and method is disclosed at page 388 of the Furber reference.

The only portion of the Furber reference relating to this portion of Applicant's claim is the "instruction prefetch unit" which discussion starts at the bottom page 387 and goes through the first six lines on page 388. Figure 14.10 is a figure of the overall "AMULET3 core organization" and the "prefetch unit" is only the top block in that figure. Furber discloses a branch prediction unit which is split into two 8-entry halves with branches at **even** half-word addresses stored in one half and branches at **odd** half-word addresses stored in the other half.

The Examiner suggests that these two halves of the branch prediction unit in Furber correspond to Applicant's "first" and "further address generation" paths. However, this suggestion contradicts the literal language of the independent claims which specify that, where a selected prefetched instruction is an instruction flow changing instruction (hereinafter "IFCI") a first address generation path determines the target address **if** one circumstance occurs and a further address generation path determines the target address **if** any other circumstance occurs, i.e., the use of the paths is asymetric. Essentially, if there is at least one IFCI, the address generation logic is used to

make the decision as to which of at least two address generation paths to follow. In claims 1, 11 and 21, the first address generation path is used "**if** the selected prefetched instruction [by definition an IFCI] is a first prefetched instruction," and the at least one further address generation path is used "**if** the selected prefetched instruction [by definition an IFCI] is one of the other prefetched instructions."

In contrast to the language of independent claims 1, 11 and 21, in Furber, any "even" half-word address is handled by the first path and any "odd" half-word address would be handled by the second path, i.e., the use of the paths is symmetric. There is no identification of the IFCI being first or not. In Furber, the decision as to the address generation path is made based upon whether the instruction is at an odd or even half word address.

The Examiner's failure to consider the detailed address generation logic language in claims 1, 11 and 21 suggests that the Examiner has misinterpreted the teaching in the Furber reference. However, should the Examiner traverse this logic, he is respectfully requested to identify where there are at least two separate address generation paths and, even more specifically, where there is any determination in Furber as to whether the selected instruction is "said first prefetched instruction." Absent such identification of claimed structure and method steps in the Furber patent, the rejection under 35 USC §103 clearly fails.

Error #2. The Furber reference does not teach "the first address generation path generating the target address more quickly than the at least one further address generation path"

Applicant's independent claims 1, 11 and 21 specifically require "the first address generation path generating the target address **more quickly** than the at least one further address generation path." (emphasis added). The Examiner alleges that this is taught in Furber at page 388, which only states "the first path takes **priority**." (emphasis added). The Examiner again

misses the claim language which states "the first address generating path generating the target address **more quickly** than" the further path (emphasis added) with no mention about priority. The Examiner provides no evidence that "priority" is the same as "more quickly."

There is no indication in Furber that any path generates a target address "more quickly" than the other, and in fact, Furber implies just the direct opposite, i.e., two 8-entry halves of the branch prediction instruction [IFCI] take the same time to operate. In fact Furber states that "a packet with a branch [IFCI] in each half word may 'hit' in both halves, whereupon the target of the first instruction (at the even address) takes priority." Thus, Furber implies the same or similar speeds, and in that event, when there is a simultaneous hit, the even address "takes priority." There is no mention of any speed or one being generated "more quickly" than the other. Applicant's claims are not directed towards **priority** of an instruction, i.e., which one to select, but rather, with respect to the generation of target address for the selected prefetched instruction and there is no suggestion in Furber that target address generation occurs **more quickly** in one path than in another path.

Because Furber clearly fails to teach this claimed aspect of Applicant's address generation logic in the prefetch unit (the top block only in Furber's Figure 14.10), there is simply no support for the Examiner's contention that this portion of Applicant's independent claims is anticipated or rendered obvious in view of the Furber reference.

Error #3. The Patterson reference is not alleged to disclose the above two features clearly missing from the Furber reference

The Examiner admits that Furber fails to teach "a pipeline stage, provided in said one further address generation path, for increasing generation speed of the target address by the first address generation path." (Final Rejection, page 3). While the Examiner alleges that Patterson

teaches speeding up execution of an address path, he does not support this with any showing that Patterson generates any one target address "more quickly" than another target address. Additionally, the Examiner does not allege that Patterson teaches deciding between two paths based upon **if** the selected prefetched instruction [IFCI] is the "first prefetched instruction" or is "one of the other prefetched instructions."

Given that the Examiner fails to allege that Patterson supplies the teachings recited above which are missing from the Furber reference, even if Furber and Patterson were combined, they would not render obvious the subject matter of independent claims 1, 11 and 21.

Error #4. The Examiner fails to identify any "reason" or "motivation" for combining the Furber and Patterson references

As noted above, even if Furber and Patterson were combined, the combination would fail to disclose or render obvious the subject matter of Applicant's independent claims 1, 11 and 21. Moreover, such combination would not obvious unless there were some "reason" or "motivation" (see the Federal Circuit decision in *In re Rouffet*, 47 USPQ2d 1453, 1457-8 (Fed. Cir. 1988)). The Examiner glosses over this glaring problem by stating that Patterson's teaching of a pipeline processor and the possibility of a higher frequency clock cycle, somehow increases execution of only the first address path but that somehow it would slow down on any other path.

There is simply no identified suggestion or teaching in Patterson that this could or would be of any use in a prefetch unit, let alone in the address generation logic within the prefetch unit as set out in Applicant's independent claims.

The Examiner makes the conclusory statement that "it would have been obvious . . . to increase the clock rate for other paths and apply it to Furber's invention." (Final Rejection, section 4, page 4). The Examiner is simply applying circular reasoning, i.e., because of his error

in ignoring the failure of Furber and Patterson to disclose all claimed elements and his imagined improvement provided by Patterson, that if Furber and Patterson were combined, they would be combined in such a fashion (as taught in the present specification) and provide the benefits of Applicant's claimed invention. This is simply not the test of obviousness and the Examiner has committed reversible error by ignoring the Federal Circuit's test of obviousness.

SUMMARY

As discussed in detail above, the Furber reference does not teach address generation logic for use only when an IFCI is present and the determination as to use of a first address generation path is made based upon **if** a "selected prefetched instruction is a first prefetched instruction." Furber also fails to contain any disclosure that there is any benefit to having the first address generation path generate a target address **more quickly** than another path. The Examiner has not indicated where the Patterson reference discloses the elements missing from Furber and, if both were combined, they would still fail to disclose the subject matter of the claims. Moreover, the Examiner has failed to provide any legal "reason" or "motivation" for combining the Furber and Patterson references and therefore has simply failed to establish any *prima facie* case of obviousness. Claims 2-10 and 12-20 depend from independent claims 1 and 11, respectively, and therefore cannot be obvious in view of the Furber/Patterson combination. Claims 7-9 and 17-19 are rejected over the Furber/Patterson/Hara combination and Hara does not supply the missing elements nor the missing "reason" or "motivation" for combining references.

As a result of the above, there is simply no support for the rejection of Applicant's independent claims 1, 11 and 21 or claims dependent thereon under 35 USC §103. Applicant respectfully requests that the Pre-Appeal Panel find that the application is allowed on the existing claims and prosecution on the merits should be closed.